A Low Noise and High Dynamic Charge Sensitive Amplifier-Shaper associated with Silicon Strip Detector for Compton Camera in hadrontherapy

M. Dahoumane, D. Dauvergne, J. Krimmer, H. Mathez, C. Ray, E. Testa, A.H. Walenta, Y. Zoccarato

A Low Noise and High Dynamic Charge Sensitive Amplifier-Shaper associated with Silicon Strip Detector for Compton Camera in hadrontherapy

M. Dahoumane, D. Dauvergne, J. Krimmer, H. Mathez, C. Ray, E. Testa, A.H. Walenta, Y. Zoccarato

***Abstract*– A 8 channel Front End Electronics (FEE) circuit has been designed and fabricated in 0.35 µm CMOS process from Austria Micro System to be coupled with the Silicon Strip Detector (SSD) of the Compton Camera for quality control of hadrontherapy. Each channel includes a Charge Sensitive Amplifier (CSA) followed by two parallel CR-RC shapers. Slow and fast shapers, with 1 µs and 15 ns shaping time, are used to measure the energy and to time stamp all events respectively. The two sides of the SSD are read thanks to a configurable system for holes and electrons. The CSA presents an open loop gain of 67 dB and 90 degrees phase margin assuring a high stability. The circuit has been successfully tested. The test results are in good agreement with analytic and simulation calculations. Here, we describe the principles and present measured performances of the prototype. A high linearity over the range of 3E3 to 3E6 electrons is reached with a conversion gain of 3.6 mV/fC. The circuit achieves an ENC (Equivalent Noise Charge) of 412 electrons rms. 75% of the total noise is generated by the small value of the feedback resistor chosen to avoid pile up phenomenon due to the 1E5 hits/s occupancy rate. A cross-talk of 2 % was measured, 99% of which is due to the power supply disturbances. The power supply dissipation is 21 mW/channel for 3.3 V supply voltage. The area of this design is 2871×1881 µm^2 including pads.**

I. Introduction

Hadrontherapy is a radiotherapy technique which consists in irradiating tumorous cells with protons or ions. During irradiation, part of the incident projectiles undergoes nuclear fragmentation and prompt-gamma rays can be used to control the ion range, because their emission profile is found to be correlated with the range, for both protons and carbon ions [1], [2]. Since excited fragments emit γ-rays almost instantaneously (below the ns range). Prompt-γ can be used to monitor online and in real-time the ion range. A Compton Camera detecting system has been proposed [3], [4] and is expected to be a very efficient and fast technique for the online dose control and high resolved 3D image reconstruction. In the proposed system shown in Fig. 1, the scatter detector is composed of a stack of 2 mm thick double-sided Silicon Strip Detectors (SSD) providing the spatial and temporal coordinates (x, y, z, t) and the energy deposited by the recoil electron during the Compton interaction of γ-rays. The scattered photon is further absorbed in a scintillator absorber.

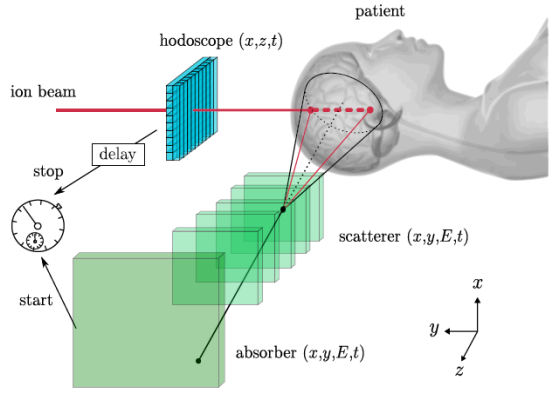

Fig. 1. Monitoring configuration system: the prompt γ-ray emission points are reconstructed by intersecting the ion trajectory, given by the hodoscope and the Compton cone, reconstructed with the Compton camera [4].

The SSD detector will be coupled with a multi-channel integrated readout electronics fulfilling the following particular requirements imposed by the application: dynamic range of 1000: 0,48 fC to 480 fC, two signal polarities readout: P and N sides of the SSD, counting rate: 1E5 hits/s, noise: ENC = 300 electrons rms, shaping Time (slow) = 1 µs for energy measurement, shaping Time (fast) =15 ns for time stamp and detector capacitance C_d = 15 pF.
For this aim, a 8-channel Front End readout Electronics (FEE) prototype is designed and fabricated using the AMS CMOS 0.35 µm process. This paper presents the design details and test results of such a prototype circuit.

II. Design Architecture

Fig. 2 illustrates a general diagram of the circuit AC-coupled with a double sided SSD detector. Each channel includes a CSA as a first stage followed by two parallel shapers. The first one, with long shaping time (1 µs), measures the input charge and optimizes the signal to noise ratio. The second one, with small shaping time (15 ns), is dedicated for timing measurement. The detector, with a capacitance C_d, produces charge pulses that are integrated on the CSA feedback capacitor C_f [5], [6]. The circuit has been designed to readout

Manuscript received November 16, 2012.
This work was supported by the ENVISION FP7 project (Grant agreement 241851), the Gamhadron ANR project, and the Rhône-Alpes research program for ion therapy.
M. Dahoumane, H. Mathez, Y. Zoccarato are with the IPNL, Université de Lyon, F-69003 Lyon, France; Université Lyon 1 and CNRS/IN2P3, UMR 5822 F-69622 Villeurbanne, France, and MICRHAU pole de MICroélectronique RHone AUvergne. (corresponding author Tel.: +33 4 26 23 44 89. e-mail: m.dahoumane@ipnl.in2p3.fr)
D. Dauvergne, J. Krimmer, , C. Ray, E. Testa, A.H. Walenta, are with with the IPNL, Université de Lyon, F-69003 Lyon, France; Université Lyon 1 and CNRS/IN2P3, UMR 5822 F-69622 Villeurbanne, France.

both P and N polarities by an appropriate feedback resistor R_f or a T resistor network. The voltage references of the shapers are selectable according to the feedback network of the CSA.

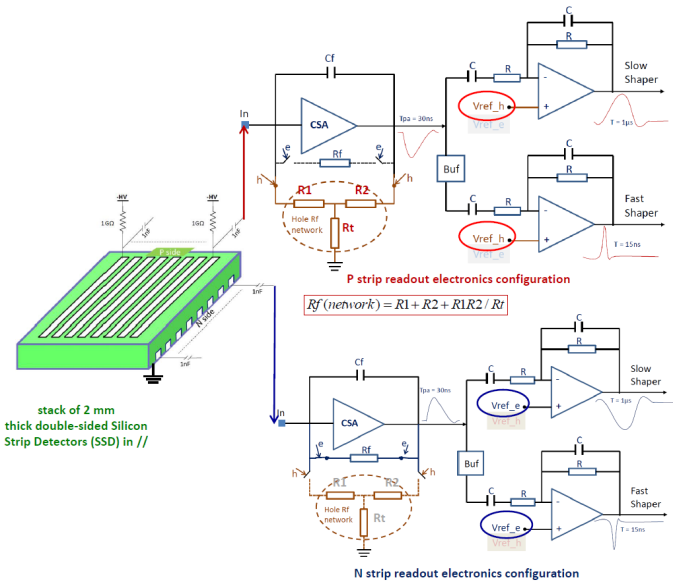

Fig. 2. General overview of the readout electronics coupled with a double sided SSD detector. The 8 strips of the SSD are AC-coupled with the 8 parallel channels of the circuit. The P and N strips are read with two different selectable configurations.

A. The Charge Sensitive Amplifier (CSA) description

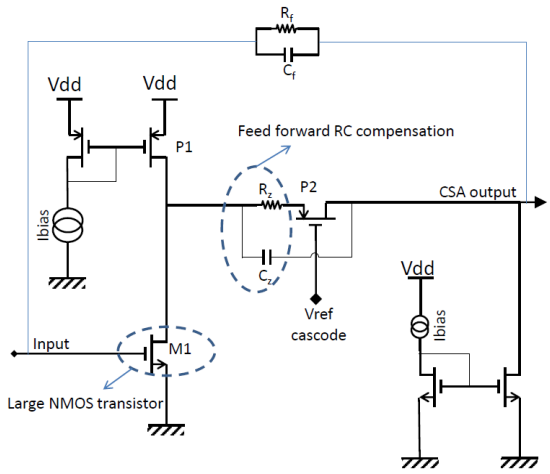

Fig. 3. The CSA architecture including RC feedback network.

Classical cascode architecture [7] has been chosen to implement the CSA stage of the readout chain as shown in Fig. 3. The geometry of each component is optimized for the foreseen performances. The first order transfer function of the CSA in response to a pulse charge stimulus is given by:

$$\frac{V_{out}}{I_{in}}(\omega) = -\frac{Zf}{1 + j\dfrac{\omega C_d}{\omega_0 G_0 C_f}} \quad , \tag{1}$$

where Z_f is the equivalent feedback impedance composed by R_f in parallel with C_f. and Cd the detector capacitance. The value of C_f (250 fC) is fixed by the maximum signal of the dynamic range and the power supply voltage value which is 3.3 V in 0.35 µm CMOS process we used. The value of the feedback resistance is chosen to discharge the feedback capacitor C_f by a time constant $\tau_{Cf} = C_f R_f$ and so to avoid the pile up phenomenon which could be caused by the high counting rate of the Compton Camera (1E5 hits/s). Thus, the small value $R_f = 4$ MΩ needed has a very harmful effect on the noise as it will be detailed in the section III.

In Fig. 3, the NMOS input transistor M1 has been chosen to get a better power supply rejection ratio and higher speed than the PMOS one. The transistor P1 is used as an active load which is mandatory for wide dynamic range such as that of our application (1000). It sets the bias current of the input transistor M1 at 5 mA from 3.3 V power supply voltage.

In order to minimize the ballistic deficit, $G_0 C_f >> C_d$, where G_0 is the open loop gain of the CSA, C_f the feedback capacitance and C_d the detector capacitance. To ensure up to 99 % of signal charge transfer, G_0 should be around 67 dB according to the following formula which gives the charge transfer rate α:

$$\alpha = \frac{1}{1 + \dfrac{C_d}{G_0 C_f}} \cdot \tag{2}$$

The rise time of the CSA output for a pulse charge stimulus is determined by the amplifier time constant τ_{CSA} as:

$$\tau_{CSA} = \frac{Cd}{2\pi f_0 G_0 C_f} = C_d R_{in} \quad , \tag{3}$$

where

$$\omega_c = 2\pi f_0 G_0 \tag{4}$$

is the Gain Bandwidth Product.

A pole–zero R and C feed forward compensation technique is used to improve stability without affecting the speed of the CSA [8]. The Bode diagram simulation of the CSA gives an open loop gain of 67 dB and a phase margin of 90°. The loop gain and Cadence STB tool simulation were also performed. The obtained results ensure high stability and very weak loss of the transferred signal charge.

The signal collected on the P strip side of the SSD has a negative shape on the CSA output. The authorized output dynamic range maintaining all transistors in the saturation mode is given by the approximate following formula:

$$V_{out} = \frac{-Q_{0\max}}{C_f} = \frac{-480\,fC}{250\,fF} = -1.92 \quad V \quad , \tag{5}$$

where Q_0 is the injected charge.

The total dynamic range corresponding to both polarities equals ±1.92 V. So, a DC level shifting is needed in the case of P polarity. For this purpose, a T resistor network is added in parallel with Rf and it is selected to read P side signals (Cf. Fig. 2). Its equivalent resistor value is given by:

$$R_{f(network)} = R_1 + R_2 + R_1 R_2 / R_t \quad . \tag{6}$$

Due to high output swing, the CSA does not include a source follower needed to increase the driving capability. This is not an issue for the complete readout chain (SCA + Shaper). However, the output signal of the CSA tested separately is slowed down and the measured gain is drastically reduced by the effect of the output load of the lines and pads.

B. The shaper implementation

A CR-RC signal shaping has been chosen to implement the two shapers. The slow shaper is directly connected to the output of the CSA while the fast one is connected through a buffering stage (Cf. Fig. 2). Active shaping is performed by using a two stage compensated Miller OTA (Operational Transconductance Amplifier). The shaping stages perform a pulse shaping primarily to optimize the signal-to-noise ratio (SNR) of the system and also to measure the energy and the time with the slow shaper around 1 µs shaping time and the fast one with a shaping time of 15 ns, respectively. Fig. 4 shows the CR-RC shaper and emphasizes the OTA architecture. The non-filtered noise of the shaper can be an issue in some cases as detailed in section III.

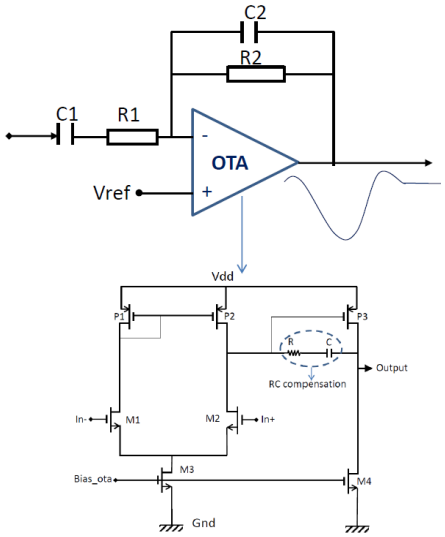

Fig. 4. Shaper scheme on the top and Miller architecture of the OTA designed to perform the shaping function in the bottom of the figure.

CR-RC shaper transfer function in the frequency domain is given by:

$$H(s) = \frac{\tau s}{(1+\tau s)^2}, \tag{7}$$

where, τ is the shaping time. Here, we chose the derivation and the integration time constants to be equal:

$$\tau_{shaping} = C_1 R_1 = R_2 C_2 . \tag{8}$$

In time domain, the gain is given by:

$$G_{SH} = \frac{R2}{R1e} . \tag{9}$$

III. NOISE STUDY

The most critical issue in this design is the noise. The desired energy resolution of the Compton camera which gives an acceptable spatial resolution of the whole hadrontherapy system must be below 1 keV. This corresponds to an input ENC (Equivalent Noise Charge) of 300 electrons rms. Fig. 5 illustrates the dominant noise sources.

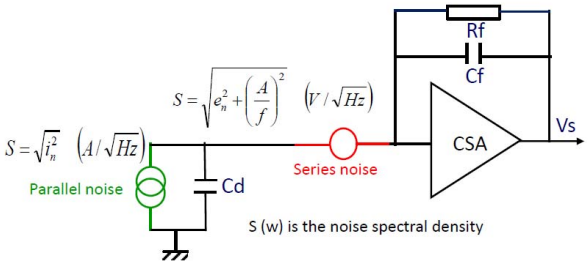

Fig. 5. Main Noise sources of a CSA.

Generally, there are two main sources of noise in a CSA: a parallel and a series noise. The parallel noise is generated by the thermal noise of the feedback resistor and the detector leakage current fluctuations. The input referred power spectral density (PSD) of the parallel noise is given by:

$$S_i(\omega) = 2qI_G + \frac{4kT}{R_f} = i_n^2 , \tag{10}$$

where, q is the electron elementary charge, I_G is the detector leakage current, k is the Boltzmann constant and T is the temperature.

The noise input voltage spectrum (series noise PSD) of a MOS transistor in saturation is given by:

$$S_v(\omega) = \frac{8}{3}\frac{kT}{g_m} + \frac{K_f}{C_{ox}WLf} = e_n^2 + \frac{A}{f} . \tag{11}$$

The first term is the channel thermal noise and the second term is the 1/f or Flicker noise [9]. Optimal noise matching is found by varying input transistor dimensions.

Total (series and parallel) noise output voltage spectrum is given by:

$$S_{out}(\omega) = \left(1 + \frac{C_d}{C_f}\right)^2 \left(e_n^2 + \frac{A}{f}\right) + \frac{i_n^{\,2}}{\omega^2 C_f^{\,2}} . \tag{12}$$

This formula is obtained through the following approximations: infinite open loop gain of CSA and considering an ideal integrator (i.e. no feedback resistance).

The output noise voltage of the complete chain is performed by integrating the product of CSA's output PSD by the shaper's Transfer function as in:

$$V_{out}^{\,2} = \int_0^\infty S_{out}(\omega)\left|H(j\omega)\right|^2 \frac{d\omega}{2\pi} . \tag{13}$$

Total input referred noise after shaping is given by:

$$ENC = e_n \frac{C_t}{\sqrt{\tau}}\frac{e}{\sqrt{8}} \oplus in\sqrt{\tau}\frac{e}{\sqrt{8}} \oplus \sqrt{\frac{K_f}{C_{ox}WL}} C_t \frac{e}{2\sqrt{\pi}} , \tag{14}$$

where C_t is the total input capacitance composed mainly by C_d and grid-source C_{gs} capacitance of the CSA input transistor, τ is the filtering time constant (shaping time).
In this design, calculations were done to find the optimal value of W/L of the input transistor leading to the best trade-off between minimizing series and 1/f noise and maintaining low value of Ct.
According to the formula (14), the dominant noise type depends on τ, C_t and the value R_f imposed by the counting rate of the physics experience. TABLE I shows a noise simulation result of the readout chain. One can see clearly that the noise due to the feedback resistor (here R_f is split into 4 resistors for layout matching) represents 75 % of the total noise.

TABLE I. NOISE SIMULATION SUMMARY: CONTRIBUTION OF VARIOUS COMPONENTS IN %

Device	Param	Noise Contribution	% Of Total	
/I57/I72/I3<0>/I55/I1/R4/R1	thermal_noise	0.000185531	36.05	RF→ 75 %
/I57/I72/I3<0>/I55/I1/R4/R2	thermal_noise	0.000115	13.85	
/I57/I72/I3<0>/I55/I1/R0/R1	thermal_noise	0.000112592	13.28	
/I57/I72/I3<0>/I55/I1/R0/R2	thermal_noise	0.000105427	11.64	
/I57/I72/I3<0>/I9/I21/R5	thermal_noise	5.67018e-05	3.37	
/I57/I72/I3<0>/I55/I0/MN4	id	5.59354e-05	3.28	Input trans (en + 1/f) →5,5 %
/I57/I72/I3<0>/I9/I22/R1	thermal_noise	5.01161e-05	2.63	
/I57/I72/I3<0>/I9/I22/MP4	id	4.94148e-05	2.56	
/I57/I72/I3<0>/I55/I0/MN4	fn	4.63033e-05	2.25	
/I57/I72/I3<0>/I9/I22/MN1	id	3.58313e-05	1.34	
/I57/I72/I38/I0/I32/MP0	id	3.53549e-05	1.31	
/I57/I72/I3<0>/I9/I22/MN2	id	3.21162e-05	1.08	
/I57/I72/I3<0>/I55/I0/MP7	id	3.04941e-05	0.97	
/I57/I72/I4/I35/MP5	id	2.5685e-05	0.69	
/I57/I72/I3<0>/I9/I22/MN16	id	2.5334e-05	0.67	
/I57/I72/I3<0>/I9/I22/MP0	id	2.38926e-05	0.60	
/I57/I72/I3<0>/I9/I21/R2	thermal_noise	2.06867e-05	0.45	
/I57/I72/I3<0>/I9/I21/R10	thermal_noise	2.06867e-05	0.45	
/I57/I72/I3<0>/I9/I21/R1	thermal_noise	2.06867e-05	0.45	
/I57/I72/I3<0>/I9/I21/R11	thermal_noise	2.06867e-05	0.45	

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000308995
No input referred noise available
The above noise summary info is for noise data

The noise of the shaper can also be a key issue in case of low gain of the shaper given by the R2/R1 ratio (Fig. 4). As we have a wide dynamic range at the output of the CSA, this ratio is fixed to 4. The global theoretical gain of the is:

$$G_{SH} = \frac{R2}{R1e} = 1.47 \cdot \quad (15)$$

The current noise in the channel of transistor P4 (Fig. 4) also generates noise in the gate through the gate-channel capacitance $C_{ox}WL$. The gate noise is due to the capacitive coupling frequency depending (f^2). The gate noise is about

$$i_g^2 = \frac{4kTg_m}{5}\left(\frac{f}{f_T}\right)^2, \quad (16)$$

$$f_T = \frac{g_m}{2\pi C_{gs}}, \quad (17)$$

where f_T is the cut off frequency of the MOSFET. This noise is important at high frequencies and is not filtered by the shaper.

IV. LAYOUT DESIGN

The multi-channel nature of the design which will fit the form of the strips of the SSD detector (crosstalk issue), low noise and high speed are parameters that require a special care when drawing the layout of the input stage (CSA).
Therefore, the R_{in} must be minimized by splitting the input transistor into a matrix of small transistors perfectly identical. The size of each channel has exactly the width of a pad (100 µm). This makes the channel multiplication easier and minimizes the mismatch between channels.
Fig. 6 shows the layout of the ASIC, an emphasis of the input transistor is carried out.

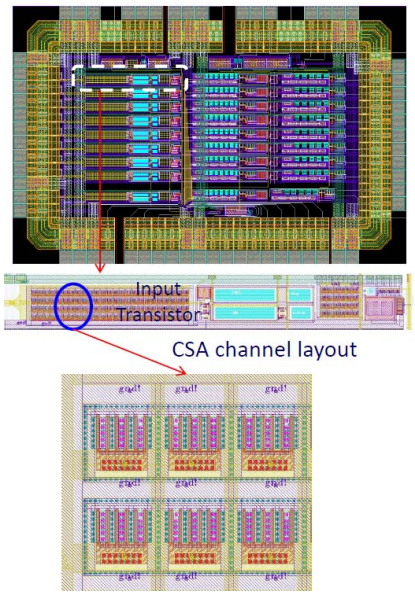

Fig. 6. Layout of the full chip fabricated in CMOS 0.35 µm process of AMS: a zoom on the CSA stage and its input transistor is shown.

V. EXPERIMENTAL RESULTS

A prototype has been fabricated in a CMOS 0.35µm process from Austria Micro System. It includes 8 channels of the described FEE readout of the Compton camera. A photography of the chip is shown in
Fig. 7.

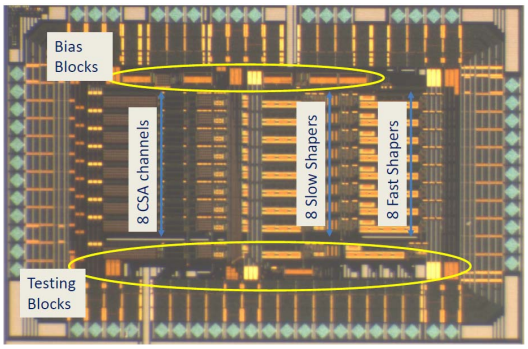

Fig. 7. Photography of the chip showing its various blocks: 8 parallel complete channels, bias blocks and individual testing blocks.

The circuit dissipates a power of 21 mW per channel from 3.3 V supply voltage and occupies an area of 2871×1881 µm^2, including pads.

A. Test setup

A test board was designed to characterize the prototype experimentally. Fig. 8 shows a photography of the test board and a synoptic of its modules. A charge injection circuit is used to simulate the detector charge which will be generated by the stopping of a Compton recoil electron in the SSD.

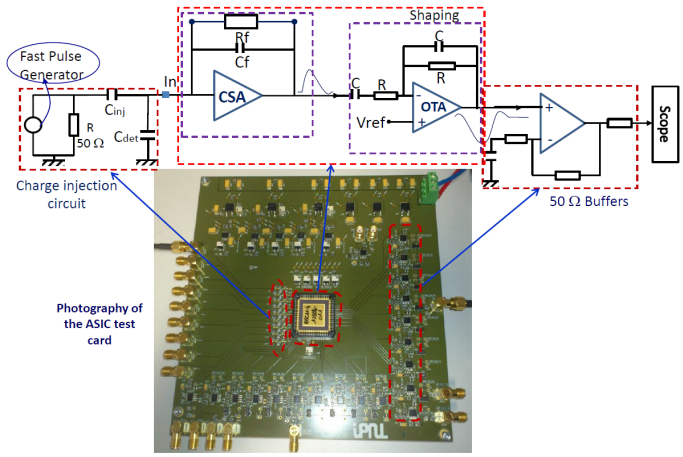

Fig. 8. Test set up and photo of the test board supporting the ASIC (device under test). On the top, is shown a synoptic of the test board.

This circuit is composed of a fast pulse generator terminated by a 50 Ω resistor, a 1 pF injection capacitor and a15 pF capacitor to simulate the detector capacitance. The response of the ASIC to an input pulse is sent to a 50 Ω buffering stage to drive different signal processing devices (e.g. scope, external amplifiers…).

B. Test results and circuit performances

The circuit has been successfully tested. The test results are in good agreement with analytic and simulation calculations. All functionalities have been validated. Fig. 9 shows outputs waveforms of the circuit for both negative and positive signal polarities. The measured shaping time of the slow shaper is 0.7 µs. However, that of the fast one (35 ns) is greater than the calculated one (15 ns). This is due to the convolution between the proper shaping time and the peaking time of the CSA (30 ns).

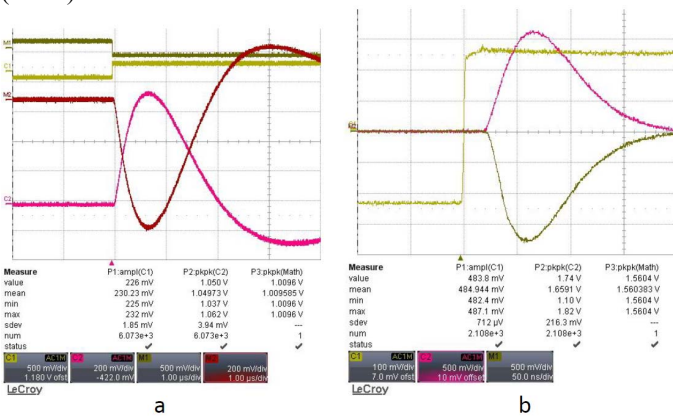

Fig. 9. Screenshot of the response of a complete chain to P and N polarities. In (a) is shown the CSA+slow shaper and in (b) CSA+fast shaper.

Linearity measurement was also performed.

The top of Fig. 10 shows the measured output and the fitted curves of the readout chain (with slow shaper) as a function of the input charge (in fC). The bottom of this figure shows the INL (Integral Non Linearity) for the two working configurations (electron on the left and hole on the right side).

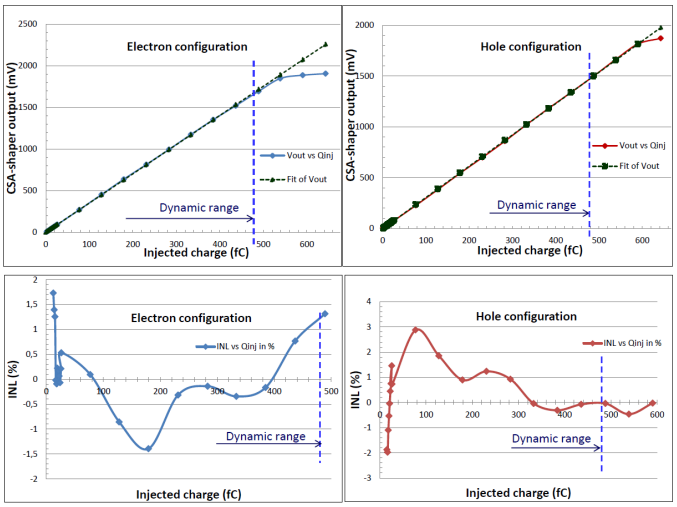

Fig. 10. Output vs. injected charge (Q_{inj}) response of a complete chain for P and N polarities on the top side. INL vs. Q_{inj} in the bottom sideof the figure.

The circuit achieves a high linearity even over the needed dynamic range, mostly less than 1 % of INL. A conversion gain of 3.6 mV/fC, very close to post layout simulation (3.9 mV/fC), is obtained up to 600 fC.

The noise evaluation has been performed according to the measurement standards. Noise and signal were measured in the same conditions (temperature and electromagnetic environment). The input referred noise ENC is obtained by:

$$ENC = \frac{V_{rms} Q_{inj}}{q V_{out}}, \qquad (18)$$

where Q_{inj} is the injected charge, q is the electron charge, V_{out} is the output voltage of the circuit corresponding to Q_{inj} and V_{rms} is the Standard Deviation which is given by:

$$Vr_{ms} = \sigma = \sqrt{\sigma^2(setup+asic) - \sigma^2(setup)}\,. \qquad (19)$$

An ENC of 412 electrons rms was measured on the channel number 1 for electron configuration. 75% of this amount comes from the combination of the feedback resistor R_f (4 MΩ) chosen to avoid the pile-up and the value of the shaping time (1µs). An ENC of 657 electrons rms is measured for the hole working mode. The performances obtained for hole configuration are slightly lower than those achieved for the electron one. This is due to the feedback network equivalent resistor used to shift the DC level in case of P polarity (Fig. 2).

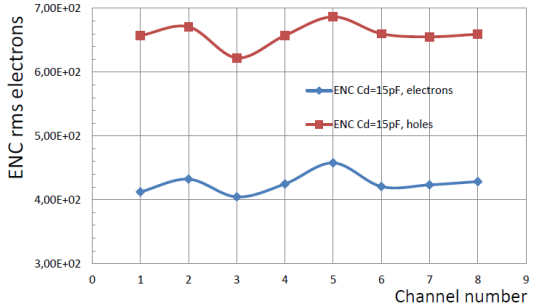

Fig. 11. ENC vs. input charge measured on all channels for electron and hole working modes.

No significant dispersion of the ENC between channels is relevant. The ENC is plotted of each channel in Fig. 11. One can see the difference between the two configurations (electron and hole).

The noise which depends on the detector capacitance was also quantified. Fig. 12 plots the calculated, schematic and post-layout simulation as well as tested curves of the ENC versus detector capacitance. The slope of the theoretical curve is very small as no additional component has been taken into account in the calculations. The slope of the tested curve is slightly higher than that of simulation. It is due to additional external noisy components such as bias resistors.

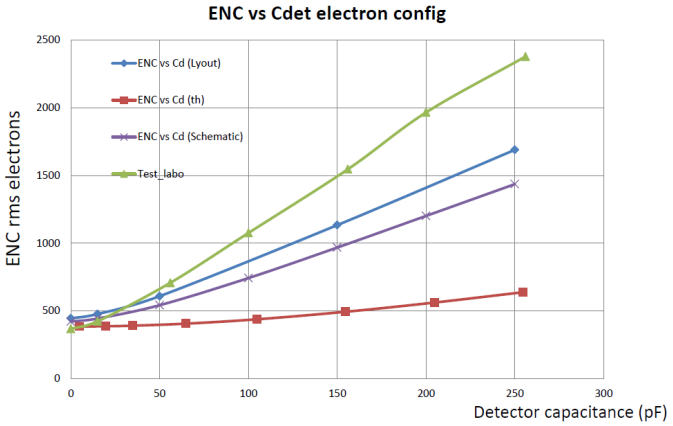

Fig. 12. Calculation, scheme and layout simulation and test ENC vs. detector capacitance.

The parallel configuration and the proximity of channels give a cross talk of ~2 % (electron mode), mostly (≥99%) coming from the supply voltage disturbance.

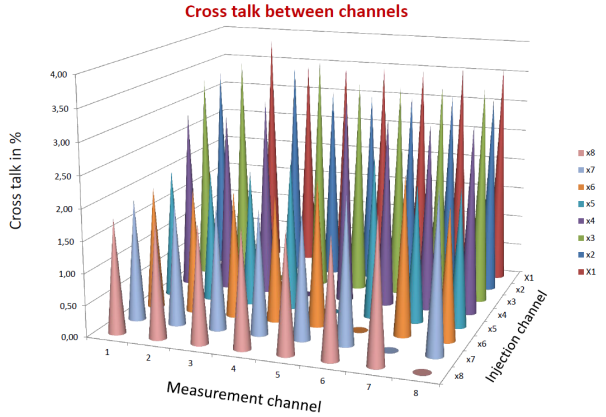

Fig. 13. Crosstalk between the CSA+Slow shaper channels measured for the electron configuration.

In Fig. 13, we injected a charge (in the left side) alternatively at the input of each single channel, and each time we measured the crosstalk on the seven other channels (front side of the figure) from the nearest to the farthest channel. The dispersion noticed on the crosstalk depends on which channel we injected the signal. It can be caused by mismatch between injection capacitors. The same crosstalk was measured for positive polarity (hole mode).

After electrical characterization, the ASIC was coupled to a 8 strip double-sided SSD detector to measure the energy spectrum of a barium radioactive source (^{133}Ba), providing photon lines at 30.9, 53, 80.9, 276, 303, 356 and 383 keV.
Fig. 14 plots the energy spectrum measured on the N strips and P strips. Note that all P strips are connected together. The measurements were performed using the ASIC on one side and using a classical electronics on the other side of the detector. An energy resolution of 8 keV FWHM has been measured for both systems. This preliminary result does not reflect the real noise of the readout electronics and the detector because of the non-optimal test environment. More precisely this is due to the length of the cables connecting strips to FEE electronics. This issue will be solved by mounting the detector and the ASIC on the same test board and thereby minimizing the length of connections and their capacitances.

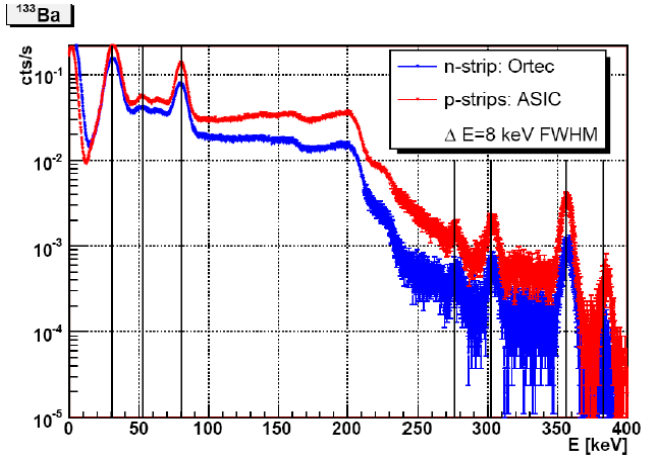

Fig. 14. Energy spectrum of the ^{133}Ba source measured with discrete electronics and the described ASIC connected to a 2mm thick 8-strip SSD (11x11 mm2 active area). P strips are connected together.

C. CSA + fast shaper chain performances

The fast shaper's branch of the chain has also been tested successfully. The test of this branch is more specific. Indeed, the charge collection time (arrival time of the signal charge at the CSA input) varies from 30 ns to 130 ns. Therefore, contrary to the slow shaper's branch which amplitude does not depend on the charge collection time, the amplitude of the fast shaper's branch depends on the collection time. This means that with the same charge, we can have different conversion gains, so making noise measurements more complicated. The area delimited by the fast shaper's output curve and the base line should be the same for a given charge, independently on the arrival time of the signal. This criterion can be used to calculate the charge at the input of the chain (CSA) after calibration. Such a measurement will be done in the next version of this circuit.
A particular care must be taken of the slew rate when designing the OTA of the fast shaper. In Fig. 15, we highlight this phenomenon. One can see the slew rate issue before enhancing the slew rate (left side of the figure); this issue disappears by enhancing the slew rate (right side of the figure). Indeed, a high slew rate is needed to drive the output load for fast shape and high dynamic signals (~35 ns shaping time in case of the fastest signal). This issue is present only in

case of falling signals which turn the output transistor of the shaper's OTA out of saturation region.

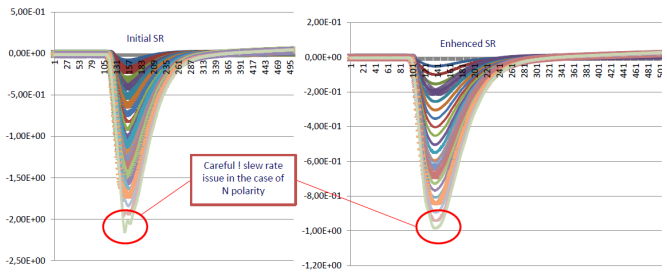

Fig. 15. Slew rate issue in case of negative, high amplitude and fast signal.

TABLE II gives a summary of the circuit performances. The measured parameters are close to schematic and post layout simulation ones. The exception of the CSA block is due the absence of a source follower stage on its output. Therefore, the gain is lowered in the test by the output load and consequently the measured input referred noise is increased. An indirect measurement of the CSA parameters using a complete chain and the gain of the slow shaper is carried out and gives results close to those of simulations.

TABLE II. PERFORMANCE SUMMARY

		Schematic	Layout	Test
Power supply		3.3 V	3.3 V	3.3 V
CSA input transistor current		5 mA	5 mA	5 mA
CSA conversion gain (mean)	electrons	3.63 mV/fC	3.41 mV/fC	2.05 mV/fC (without SF)
	holes	3.55mV/fC	3.31 mV/fC	1,88 mV/fC (without SF)
CSA Noise (ENC) rms	electrons	502 e- rms	524.37 e- rms	835,85 e- rms
	holes	577.5 e- rms	616.3 e- rms	1186,1 e- rms
CSA-Slow Shaper conversion gain	electrons	4.35 mV/fC	3.91 mV/fC	3.6 mV/fV
	holes	3.85 mV/fC	3.45 mV/fC	3 mV/fC
CSA-Slow Shaper Noise (ENC) rms	electrons	443.95 e- rms	475.37 e- rms	412e- rms
	holes	642.85 e- rms	674.11 e- rms	657 e- rms
Shaping Time (slow shaper)	electrons	0.7 us	0.9 us	0,7 us

VI. CONCLUSION AND UPCOMING WORK

In order to read out the signals delivered by the Silicon Strip Detectors constituting the Compton camera for prompt-gamma monitoring of hadrontherapy, a 8 channel front end readout electronics has been designed and fabricated in 0.35 µm CMOS process from AMS. Each channel is built of a Charge Sensitive Amplifier (CSA) connected to two parallel shapers slow and fast. Exhaustive tests were performed and all the functionalities of the above-described circuit have been validated. The series noise of this design was minimized to ~5% of the total noise thanks to high optimization of the input transistor. In the future version of this circuit, we will replace the feedback resistor by a MOS switch and thus eliminate nearly 75% of the total noise. Also, further functionalities will be integrated such as a comparator providing a logic level for time stamp, multiple shaping and multiple gain.

ACKNOWLEDGMENT

First, we would thank Mr. E. Bechetoille for his very useful technical help. We would also like to thank Mr. D. Delaunay and Mr. R. Della Negra for their contribution on the test of this circuit.

REFERENCES

[1] C.-H. Min, C. H. Kim, M.-Y. Youn, et J.-W. Kim, « Prompt gamma measurements for locating the dose falloff region in the proton therapy », Appl. Phys. Lett., vol. 89, no. 18, p. 183517-3, oct. 2006.

[2] E. Testa, M. Bajard, M. Chevallier, D. Dauvergne, F. Le Foulher, N. Freud, J.-M. Létang, J.-C. Poizat, C. Ray, et M. Testa, « Monitoring the Bragg peak location of 73 MeV/u carbon ions by means of prompt γ-ray measurements », Appl. Phys. Lett., vol. 93, no. 9, p. 093506, 2008.

[3] M.-H. Richard, M. Chevallier, D. Dauvergne, N. Freud, P. Henriquet, F. Le Foulher, J. M. Létang, G. Montarou, C. Ray, F. Roellinghoff, E. Testa, M. Testa, et A. H. Walenta, « Design Guidelines for a Double Scattering Compton Camera for Prompt-gamma imaging During Ion Beam Therapy: A Monte Carlo Simulation Study », IEEE Transactions on Nuclear Science, vol. 58, no. 1, p. 87-94, févr. 2011.

[4] F. Roellinghoff, M.-H. Richard, M. Chevallier, J. Constanzo, D. Dauvergne, N. Freud, P. Henriquet, F. Le Foulher, J. M. Létang, G. Montarou, C. Ray, E. Testa, M. Testa, et A. H. Walenta, « Design of a Compton camera for 3D prompt-gamma imaging during ion beam therapy », Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, vol. 648, no. Supplement 1, p. S20-S23, août 2011.

[5] Paul O'Connor and Gianluigi De Geronimo, "Prospects for charge sensitive amplifiers in scaled CMOS", Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, Volume 480, Issues 2–3, 21 March 2002, Pages 713–725.

[6] R. Hofmann and G. Lutz, "Development of readout electronics for monolithic integration with diode strip detectors", Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, Volume 226, Issue 1, 15 September 1984, Pages 196–199.

[7] V. Radeka, P. Rehak et al., "Design of a charge sensitive preamplifier on high resistivity silicon," IEEE Trans. Nuclear Science, vol.35, no.1, pp.155-159, Feb. 1988

[8] W. Sansen and Z. Y. Chang, "Feedforward Compensation techniques for High Frequency CMOS amplifier", IEEE J. Solid-State Circ., vol. 25, N°6, pp.1590-1595, December 1990.

[9] W.M.C Sansen and Z.Y. Chang, "Limits of low noise performance of detector readout front ends in CMOS technology", IEEE Transactions on Circuits and Systems, Volume: 37 , Issue: 11 Nov 1990 Page(s): 1375 – 1382.